What is claimed is:

1. An article comprising:

a storage medium having stored therein a memory array, said memory array comprising a programmable data element, and said storage medium also having stored therein instructions that when executed by a machine result in the following:

analyzing data in a location of said memory array, said location associated with a predetermined frame type of a received frame;

receiving an input signal indicating if said received frame contains an error; and

providing an output signal indicating a negative receive response status if said input signal indicates an error in said received frame.

2. The article of claim 1, wherein said instructions that when executed by said machine also result in the following:

checking a state of a first check bit in said location of said memory array associated with said predetermined frame type, wherein a state of said first check bit indicates if said predetermined frame type is supported; and

providing said output signal indicating said negative receive response status if said state of said first check bit is in a first state.

3. The article of claim 2, wherein said programmable data element comprises said first check bit.

4. The article of claim 2, wherein said instructions that when executed by said machine also result in the following:

checking a state of a second check bit in said location of said memory array associated with said predetermined frame type;

comparing count data for said received frame with a frame length in said location of said memory associated with said predetermined frame type if said state of said second check bit is in a first state; and

providing said output signal indicating said negative receive response status if said count data is different than said frame length.

5. The article of claim 4, wherein said programmable data element comprises said second check bit and said frame length.

6. A system comprising:

a circuit card comprising an integrated circuit, said circuit card being capable of being coupled to a bus, said integrated circuit comprising a storage medium having stored therein a memory array, said memory array comprising a programmable data element, and said storage medium also having stored therein instructions that when executed by a machine result in the following:

analyzing data in a location of said memory array, said location associated with a predetermined frame type of a received frame;

receiving an input signal indicating if said received frame contains an error; and

providing an output signal indicating a negative receive response status if said first input signal indicates an error in said received frame.

7. The system of claim 6, wherein said instructions that when executed by said machine also result in the following:

checking a state of a first check bit in said location of said memory array associated with said predetermined frame type, wherein a state of said first check bit indicates if said predetermined frame type is supported; and

providing said output signal indicating said negative receive response status if said state of said first check bit is in a first state.

8. The system of claim 7, wherein said programmable data element comprises said first check bit.

9. The system of claim 7, wherein said instructions that when executed by said machine also result in the following:

checking a state of a second check bit in said location of said memory array associated with said predetermined frame type;

comparing count data for said received frame with a frame length in said location of said memory associated with said predetermined frame type if said state of said second check bit is in a first state; and

providing said output signal indicating said negative receive response status if said count data is different than said frame length.

10. The system of claim 9, wherein said programmable data element comprises said second check bit and said frame length.

11. A method comprising:

receiving a frame;

determining a frame type of said frame;

accessing a location of memory associated with said frame type, said location comprising at least one programmable data element; and

checking a validity of said frame in response to data in said location of memory associated with said frame type.

12. The method of claim 11, wherein said programmable data element comprises a check bit indicating if said frame type is supported, and wherein said checking said validity of said frame comprises providing an output signal indicating a negative receive response status if said check bit is in a first state.

13. The method of claim 11, further comprising:

counting data in said frame; and

comparing count data of said frame from said counting operation with a frame length in said location of memory associated with said frame type, and wherein said checking said validity of said frame comprises providing an output signal indicating a negative receive response status if said count data is different from said frame length.

14. The method of claim 13, wherein said frame length comprises a maximum frame length and wherein said checking said validity of said frame comprises providing an output signal indicating a negative receive response status if said count data is greater than said maximum frame length.

15. The method of claim 11, further comprising:

receiving a first set up frame specifying a first frame type and a first frame length;

storing said first frame length in a location of memory associated with said first frame type;

receiving a second data frame immediately after said first set up frame; and

checking a validity of said second data frame in response to data in said location of memory associated with said first frame type from said first set up frame.

16. The method of claim 15, wherein said checking said validity of said second data frame comprises providing an output signal indicating a negative receive response status if a length of said second data frame is different than said first frame length.

17. The method of claim 15, wherein said first set up frame comprises a programmed input/output (PIO) Setup Frame Information Structure (FIS) and said second data frame comprises a data FIS.

18. An apparatus comprising:

circuitry capable of receiving a frame, determining a frame type of said frame, accessing a location of memory associated with said frame type, said location comprising at least one programmable data element; and checking a validity of said frame in response to data in said location of memory associated with said frame type.

19. The apparatus of claim 18, wherein said programmable data element comprises a check bit indicating if said frame type is supported, and wherein said checking said validity of said frame comprises providing an output signal indicating a negative receive response status if said check bit is in a first state.

20. The apparatus of claim 18, wherein said circuitry is further capable of counting data in said frame, and comparing count data of said frame from said counting operation with a frame length in said location of memory associated with said frame type, and wherein said checking said validity of said frame comprises providing an output signal indicating a negative receive response status if said count data is different from said frame length.

21. The apparatus of claim 20, wherein said frame length comprises a maximum frame length and wherein said checking said validity of said frame comprises providing an output signal indicating a negative receive response status if said count data is greater than said maximum frame length.

22. The apparatus of claim 18, wherein said circuitry is further capable of receiving a first set up frame specifying a first frame type and a first frame length, storing said first frame length

in a location of memory associated with said first frame type, receiving a second data frame immediately after said first set up frame; and checking a validity of said second data frame in response to data in said location of memory associated with said first frame type from said first set up frame.

23. The apparatus of claim 22, wherein said checking said validity of said second data frame comprises providing an output signal indicating a negative receive response status if a length of said second data frame is different than said first frame length.

24. The apparatus of claim 22, wherein said first set up frame comprises a programmed input/output (PIO) Setup Frame Information Structure (FIS) and said second data frame comprises a data FIS.